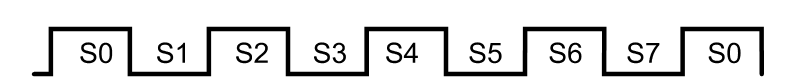
Read Cycle 68000 with 8MHz from EEPROM 28C64



Valid Address

A

UDS/LDS

R/W

D

Valid Data

: Memory access time, the time between address valid and data valid. : Data setup time.

: Address become valid (Clock Low to Address Valid)

3 =

**Without** critical speed path (logic gates) the Memory Access time**:**

=

=

**With** critical speed path (logic gates) the Memory Access time:

Three logical gates cause delay; two NANDS and one NOR.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| NAND |  |  | NOR |  |  |
| MAX | 22 | 15 | MAX | 22 | 15 |
| MIN | 00 | 00 | MIN | 00 | 00 |

We are interested in the Pulse High to Low in both gates, and the maximum delay caused is 66ns

Therefore,

=

= And the memories Maximum access time is 250ns therefore, it’s safe.